AF & IFW

Docket No.: GR 97 P 1903

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MAIL STOP: APPEAL BRIEF-PATENTS

By: Yonghong Chen Date: June 3, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	09/483,737 Confirmation No.: 8769
Inventor	:	Hansjörg Reichert
Filed	:	January 14, 2000
Title	:	Method and Apparatus for Producing a Chip-Substrate Connection
TC/A.U.	:	2826
Examiner	:	Ahmed N Sefer
Customer No.	:	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated January 12, 2005, finally rejecting claim 15.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $500.00 to cover the fee for filing the *Brief on Appeal*.

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Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

There are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claim 15 is rejected and is under appeal. Claims 2-8 were cancelled in an amendment dated October 25, 2004. Claims 11-14 and 16 were cancelled in an amendment dated January 24, 2002. Claim 17 was cancelled in an amendment dated April 11, 2003. Claims 1 and 9-10 were withdrawn from consideration.

Status of Amendments:

No claims were amended after the final Office action. *A Notice of Appeal* was submitted on April 7, 2005.

Summary of the Claimed Subject Matter:

The invention of the instant application relates to a semiconductor component. The semiconductor component includes

a solder containing at least two components with at least two metal-containing constituents including a first constituent X being formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved in materials which are to be joined. See page 1, lines 12-16 of the specification. The solder has a hypereutectic concentration of the second constituent Y. See page 7, lines 24-26 of the specification. The semiconductor component further includes a substrate (2) and a semiconductor chip (1) having a rear side and an adhesive or diffusion barrier (4) provided on the rear side. The semiconductor chip is secured at the rear side of the semiconductor chip to the substrate by alloying or brazing using the solder to form a chip-substrate connection by the solder. See page 8, line 23 to page 9, line 5 of the specification as well as Figs. 2A and 2B. The solder contains a gold-tin compound (AuSn) having a composition by weight of Au to Sn of 70 to 30 and forming a layer having a thickness of from about 1 μm to about 2 μm. See page 6, lines 5-10 and page 9, line 7 of the specification.

References Cited:

JP 6-291239	Yamagishi	October 18, 1994
JP 6-326210	Ishii	November 25, 1994

5,234,153 Bacon et al. August 10, 1993

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claim 15 is obvious over Yamagishi in view of Ishii and Bacon et al. under 35 U.S.C. §103(a).

Grouping of Claims:

Claim 15 is independent.

Argument:

Whether or not claim 15 is obvious over Yamagishi in view of Ishii and Bacon et al. under 35 U.S.C. §103(a).

In item 3 on pages 2-3 of the above-mentioned Office action, claim 15 has been rejected as being unpatentable over Yamagishi et al. in view of Ishii and Bacon et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 15 calls for, inter alia:

> said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder.

The Examiner has stated that Yamagishi et al. disclose in Fig. 1 (C) a semiconductor chip 4 secured to the substrate by one of alloying and brazing using the solder (see the fourth paragraph on page 2 of the final Office action). This statement is incorrect. Yamagishi et al. do not disclose a chip-substrate connection by a solder. As can be clearly seen in Fig. 1(C) of Yamagishi et al., there is no solder between the chip 4 and the substrate 1. Rather, a solder is only applied between the housing 5 and the substrate 1 and between the pin bearing pad 3 and the lead pin 2.

Ishii discloses a sub-mount interposed between a laser chip 1 and a metal block 5. As can be seen from Fig. 2 of Ishii, the chip 1 and the substrate 40 do not form a chip-substrate connection by a solder. Rather, there is a barrier layer 7a between the chip 1 and the substrate 40. It is noted that in the invention of the instant application the adhesive or diffusion barrier (4) provided on the rear side of the semiconductor chip is part of the semiconductor chip, not a separate layer as shown in Fig. 2 of Ishii. Therefore, Ishii also does not teach a chip-substrate connection by solder between the rear side of the semiconductor chip and the substrate. Rather, Ishii only shows a chip-barrier layer connection by the solder.

The reference Bacon et al. has not been cited by the Examiner as disclosing a chip-substrate connection by a solder. Rather, it was cited by the Examiner as teaching the advantages of using a thin gold-tin compound solder. In fact, Bacon et al. also do not disclose a chip-substrate connection as recited in claim 15 of the instant application.

Clearly, none of the cited references shows "said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder," as recited in claim 15 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art.

In view of the foregoing, the honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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YC/bb

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Claims Appendix:

15. A semiconductor component, comprising:

a solder containing at least two components with at least two metal-containing constituents including a first constituent X being formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved in materials which are to be joined, and said solder having a hypereutectic concentration of said second constituent Y;

a substrate; and

a semiconductor chip having a rear side and an adhesive or diffusion barrier provided on said rear side;

said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder;

said solder containing a gold-tin compound (AuSn) having a composition by weight of Au to Sn of 70 to 30 and forming a layer having a thickness of from about 1 μm to about 2 μm.

Evidence Appendix:

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

Since there are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, no copies of decisions rendered by a court or the Board are available.